Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCIIONS:**

1. **D1**
2. **S1**
3. **NC**
4. **NC**
5. **IN1**
6. **NC**
7. **GND**
8. **V –**
9. **NC**
10. **NC**
11. **NC**
12. **S2**
13. **D2**
14. **V +**

**.088”**

**.087”**

**DIE ID**

**B**

**1 14 13**

**6 7 8**

**12**

**11**

**10**

**9**

**2**

**3**

**4**

**5**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .087” X .088” DATE: 2/9/17**

**MFG: SILICONIX THICKNESS .014” P/N: DG300A**

**DG 10.1.2**

#### Rev B, 7/19/02